WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a memory cell array including plural memory cells;

an input/output circuit inputting plural bits of serial data from outside and outputting the plural bits of serial data to outside;

a register section comprising a first register and a second register, the first register receiving the plural bits of serial data from the input/output circuit and converting the plural bits of serial data into parallel data, the second register receiving plural bits of parallel data from the plural memory cells and converting the plural bits of parallel data into serial data; and

a signal generating circuit generating plural first control signals and plural second control signals, the plural first control signals supplying a conversion timing for each bit when the plural bits of serial data are converted into the parallel data, the plural second control signals supplying a conversion timing for each bit when the plural bits of parallel data are converted into the serial data, the signal generating circuit controlling a timing of one of rise and fall of the plural first control signals and sets which of the plural memory cells should store a value for each bit, of the plural bits of serial data, and controlling a timing of one of rise and fall of the plural second control signals and sets which number of value of the serial data should be the value for each bit, of the plural bits of parallel data read from the plural memory cells.

2. The semiconductor memory device according to claim 1, wherein the first register is composed of a first write register receiving even numbers of data, of the plural bits of serial data, and converting the even numbers of data into parallel data, and a second write register receiving odd numbers of data, of the plural bits of serial data, and converting the odd numbers of data into parallel data; and

the second register is composed of a first read register receiving even numbers of data, of the plural bits of parallel data, and converting the even numbers of data into serial data, and a second read register receiving odd numbers of data, of the plural bits of parallel data, and converting the odd numbers of data into serial data.

3. The semiconductor memory device according to claim 2, wherein the first write register comprises plural transfer gates, even numbers of data, of the plural bits of serial data, are input to an end of a current path of each of the plural transfer gates, the first control signals are input to gates of the plural transfer gates, respectively; and

the second write register comprises plural transfer gates, odd numbers of data, of the plural bits of serial data, are input to an end of a current path of each of the plural transfer gates, the first control signals are input to gates of the plural transfer gates, respectively.

4. The semiconductor memory device according to claim 2, wherein the first read register comprises plural transfer gates, even numbers of data, of the plural bits of parallel data, are input to an end of a current path of each of the plural transfer gates, respectively, the second control signals are input to gates of the plural transfer gates, respectively; and

the second read register comprises plural transfer gates, odd numbers of data, of the plural bits of parallel data, are input to an end of a current path of each of the plural transfer gates, respectively, the second control signals are input to gates of the plural transfer gates, respectively.

5. The semiconductor memory device according to claim 3, wherein the first read register comprises plural transfer gates, even numbers of data, of the plural bits of parallel data, are input to an end of a current path of each of the plural transfer gates, respectively, the second control signals are input to gates of the plural transfer gates, respectively; and

the second read register comprises plural transfer gates, odd numbers of data, of the plural bits of parallel data, are input to an end of a current path of each of the plural transfer gates, respectively, the second control signals are input to gates of the plural transfer gates, respectively.

6. The semiconductor memory device according to claim 3, wherein the first control signals that are input to the first write register are common to the first control signals that are input to the second write register.

7. The semiconductor memory device according to claim 4, wherein the second control signals that are input to the first read register are common to the second control signals that are input to the second read register.

8. The semiconductor memory device according to claim 1, wherein the first control signals and the second control signals that are generated by the signal generating circuit are common to each other.

9. The semiconductor memory device according to claim 5, wherein the first control signals that are input to the first write register and the second write register are common to the second control signals that are input to the first read register and the second read register.

10. The semiconductor memory device according to claim 1, wherein each of the plural first control signals that are output from the signal generating

circuit has any one of a different leading edges and a different trailing edges.

11. The semiconductor memory device according to claim 1, wherein at least two of the plural first control signals that are output from the signal generating circuit have any one of the same rise edge and the same fall edge.

12. The semiconductor memory device according to claim 6, wherein the common signals are input to the first write register and the second write register after decoded with a predetermined signal.

13. The semiconductor memory device according to claim 7, wherein the common signals are input to the first read register and the second read register after decoded with a predetermined signal.

14. The semiconductor memory device according to claim 8, wherein the common signals are input to the first register and the second register after decoded with a predetermined signal.

15. The semiconductor memory device according to claim 9, wherein the common signals are input to the first write register, the second write register, the first read register, and the second read register after decoded with a predetermined signal.